

4

3

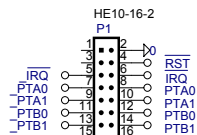
2

1

B

B

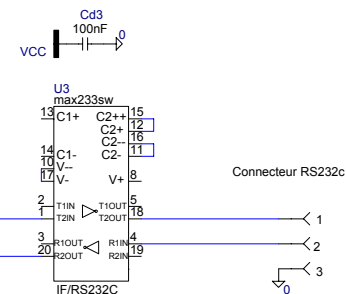
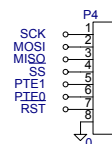
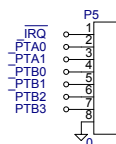
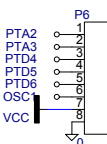
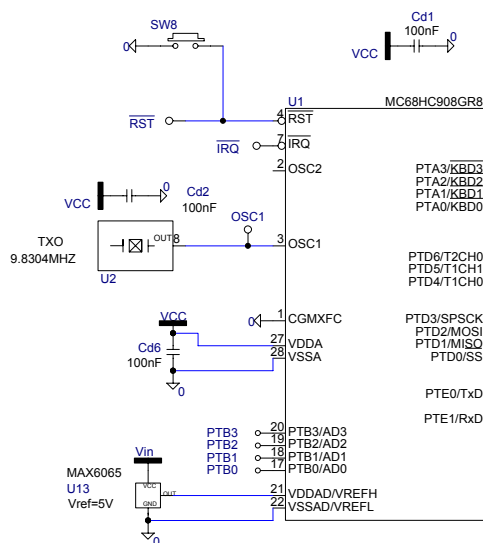
In-system Programming



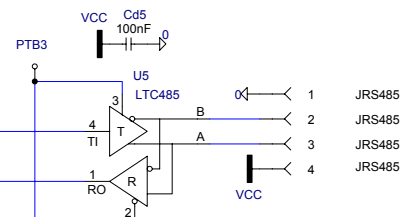
NOTES:

Monitor Mode Entry (external clock)

- IRQ à VTST
- RESET à VDD
- PTA1 à '0'
- PTA0 à '1' voir sonde ISP
- PTB0 à '1'
- PTB1 à '0'

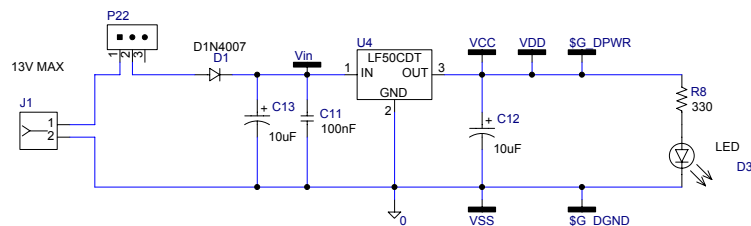


Connecteur RS485



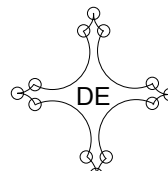
A

A



MYTBLK-A/B/C/G

ACADEMIE



TOULOUSE

LYP CHAMPOLLION avenue Pezet 46100 FIGEAC

KIT 68HC908GR8

SIZE	BTS	DESSINATEURS	REV
B	Electronique	DALET	1
SCALE: 1	DATE: 16/12/2003	SHEET	1 OF 1

4

3

2

1

15/12/2003

